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EXAMINER	
SAVLA, ARPAN P	

ART UNIT	PAPER NUMBER
2185	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/631,185	CHAUVEL ET AL.	
	Examiner	Art Unit	
	Arpan P. Savla	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 December 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *7,9,10,15 and 16* is/are allowed.

6)☒ Claim(s) *1-6,8,11-14 and 17-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

This Office action is in response to Applicant's communication filed December 17, 2007 in response to the Office action dated August 22, 2006. Claims 1, 7, 9, 15, and 16 have been amended. Claims 1-20 are pending in this application.

OBJECTIONS

Specification

1. In view of Applicant's amendment, the objections to the specification have been withdrawn.

REJECTIONS NOT BASED ON PRIOR ART

Claim Rejections - 35 USC § 112

2. In view of Applicant's amendment, the 112 rejections to **claims 1-10** have been withdrawn.

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-4, 8, 11, and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Shen et al. (U.S. Patent 5,687,336) (hereinafter "Shen").

5. **As per claim 1**, Shen discloses a method of managing memory, comprising:

determining stack trend information using current and future stack operating instructions (col. 4, lines 11-15 and 36-60; Fig. 2; col. 3, line 65 – col. 4, line 7; col. 6, line 58 – col. 7, line 15; Fig. 4); *It should be noted that Shen's final value for the stack pointer indicates whether the stack size has increased or decreased.*

utilizing the trend information to reduce data traffic between various levels of a memory (col. 8, lines 34-47). *It should be noted that by having the stack pointer signal a mis-aligned access, push/pop pairing is prevented, a second cache access is prevented, thus, data traffic between various levels of the cache are reduced.*

6. **As per claim 2**, Shen discloses determining the trend information includes examining future instructions to determine if the size of the stack is going to decrease as a result of future instructions (col. 3, line 65 – col. 4, line 7; col. 4, lines 11-15 and 36-60; col. 5, lines 1-5 and 9-10; Figs. 2 and 4).

7. **As per claim 3**, Shen discloses a predetermined number of instructions are used in determining stack trend information (col. 3, lines 65-67; col. 6, lines 47-48). *It should be noted that if there is only one instruction per stage and there are five stages in the pipeline, then five instructions are used in determining stack trend information.*

8. **As per claim 4**, Shen discloses the number of predetermined instructions is at least two (col. 3, lines 65-67; col. 6, lines 47-48). *See citation note for claim 3 above.*

9. **As per claim 8**, Shen discloses determining the trend information includes examining future instructions to determine if the size of the stack is going to increase as a result of future instructions (col. 3, line 65 – col. 4, line 7; col. 4, lines 11-15 and 36-60; col. 5, lines 1-7; Figs. 2 and 4).

10. **As per claim 11**, Shen discloses a computer system, comprising:

a processor (col. 4, line 37; Fig. 2);

a memory coupled to the processor (col. 4, lines 33-34; Fig. 2, element 26); *It should be noted that the memory physically lies within the processor, thus making the memory and processor coupled.*

a stack that exists in memory and contains stack data (col. 4, lines 33-34; Fig. 2, element 26);

a memory controller coupled to the memory (col. 5, lines 19-23). *It should be noted that Shen does not expressly disclose a memory controller in the design. However, the citation noted above discloses reading from and writing to a cache memory. As one of ordinary skill in the art knows a memory controller is inherently required to interface with any memory.*

trend logic (col. 4, lines 40-43; Fig. 2, element 20);

wherein the processor executes instructions (col. 4, lines 36-37);

wherein the trend logic provides trend information about the stack to the controller (col. 5, lines 10-14 and 19-22; Fig. 2, elements 20, 24, 40, and 94); *It should noted that the trend information is calculated by the three-way addition of the stack pointer, segment base, and increment value (which comes from the increment logic)*

and then the trend information is sent from the three-port adder to the memory controller.

wherein the trend information about the stack is based on at least one future instruction (col. 3, line 65 – col. 4, line 7; col. 4, lines 11-15 and 36-60; Figs. 2 and 4).

11. **As per claim 13**, Shen discloses the trend logic determines a net stack trend based on current instruction and future instruction information coming from the decode logic (col. 3, line 65 – col. 4, line 7; col. 4, lines 11-15; col. 4, lines 36-60; Fig. 2, elements 20, 30, and 94).

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claim 5 is rejected under 35 U.S.C. 103(a) as being obvious over Shen et al. in view of Ebrahim et al. (U.S. Patent 5,893,121) (hereinafter "Ebrahim").

14. Shen discloses all the limitations of claim 5 except the cache memory maintains a single dirty cache line for stack data.

Ebrahim discloses the cache memory maintains a single dirty cache line for stack data (col. 5, lines 32-35). *It should be noted that a cache block maintaining a dirty bit is analogous to a "dirty cache line".*

Shen and Ebrahim are analogous art because they are from the same field of endeavor, that being stack memory.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use Ebrahim's stack cache memory containing a single dirty cache line within Shen's stack trend tracker system.

The motivation for doing so would have been to avoid writing back unmodified stack cache blocks to main memory (Ebrahim, col. 5, lines 33-35).

Also, at the time of the invention it would have been obvious to a person of ordinary skill in the art to apply Ebrahim's stack cache memory containing a single dirty cache line to Shen's stack trend tracker system because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded the predictable results of automatically recovering memory objects no longer in use by the operating system and application programs in a computer system.

Therefore, it would have been obvious to combine Ebrahim with Shen for the benefit of obtaining the invention as specified in claim 5.

15. Claims 6 and 17-20 are rejected under 35 U.S.C. 103(a) as being obvious over Shen et al. in view of Steely et al. (U.S. Patent 6,801,986) (hereinafter "Steely").

16. **As per claim 6**, Shen discloses all the limitations of claim 6 except determining which word of the dirty cache line is going to be written to.

Steely discloses determining which word of the dirty cache line is going to be written to (col. 2, lines 39-43). *It should be noted that when taking the broadest reasonable interpretation of the claim language it is clear that the limitations of the claim do not specify how many words are in a dirty cache line. Steely does not disclose the exact size of a cache line, however, at minimum it must contain one word, meaning a write request would always go to a predetermined word with a dirty cache line, that being the only word in the dirty cache line.*

Shen and Steely are analogous art because they are from the same field of endeavor, that being computer memory systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use Steely's dirty cache line write procedure with Shen's stack trend tracker system.

The motivation for doing so would have been to produce an atomic read/write sequence which reduces the number of system commands and so reduces system overhead during contention for a memory block by two or more processors in a multiprocessor computer system (Steely, col. 6, lines 14-18). *See col. 2, lines 46-49 for a definition of an "atomic read/write."*

Also, at the time of the invention it would have been obvious to a person of ordinary skill in the art to apply Steely's dirty cache line write procedure to Shen's stack trend tracker system because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods

with no change in their respective functions, and the combination would have yielded the predictable results of livelock prevention.

Therefore, it would have been obvious to combine Steely with Shen for the benefit of obtaining the invention as specified in claim 6.

17. **As per claim 17**, Shen discloses a method, comprising:

determining whether the size of a stack is increasing or decreasing (col. 3, line 65 – col. 4, line 7; col. 4, lines 11-15 and 36-60; col. 5, lines 1-7 and 9-10; Fig. 2).

Shen does not expressly disclose issuing a write request to a cache memory, wherein the cache memory includes multiple cache lines;

determining whether the write request refers to a predetermined word within a dirty cache line.

Steely discloses issuing a write request to a cache memory, wherein the cache memory includes multiple cache lines (col. 1, lines 51-52, col. 9, lines 61-62; Fig. 2A, element 221); *It should be noted that the presence of probe commands and cache tags indicate the cache memory has multiple cache lines.*

determining whether the write request refers to a predetermined word within a dirty cache line (Steely, col. 2, lines 39-43); *It should be noted that when taking the broadest reasonable interpretation of the claim language it is clear that the limitations of the claim do not specify how many words are in a dirty cache line. Steely does not disclose the exact size of a cache line, however, at minimum it must contain one word, meaning a write request would always go to a predetermined word with a dirty cache line, that being the only word in the dirty cache line.*

Shen and Steely are analogous art because they are from the same field of endeavor, that being computer memory systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use Steely's dirty cache line write procedure with Shen's stack trend tracker system.

The motivation for doing so would have been to produce an atomic read/write sequence which reduces the number of system commands and so reduces system overhead during contention for a memory block by two or more processors in a multiprocessor computer system (Steely, col. 6, lines 14-18). *See col. 2, lines 46-49 for a definition of an "atomic read/write."*

Also, at the time of the invention it would have been obvious to a person of ordinary skill in the art to apply Steely's dirty cache line write procedure to Shen's stack trend tracker system because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded the predictable results of livelock prevention.

Therefore, it would have been obvious to combine Steely with Shen for the benefit of obtaining the invention as specified in claim 17.

18. **As per claim 18**, the combination of Shen/Steely discloses determining whether the write request will be to the end of a dirty cache line (Steely, col. 8, lines 55-57; Fig. 2A, element 221). *It should be noted that when taking the broadest reasonable interpretation of the claim language it is clear that the limitations of the claim do not*

specify how many words are in a dirty cache line. Steely does not disclose the exact size of a cache line, however, at minimum it must contain one word, meaning a write request would always write bits to both the beginning and end of a dirty cache line.

19. **As per claim 19**, the combination of Shen/Steely discloses the stack size is increasing (Shen, col. 5, lines 5-7) and the dirty cache line is written to a main memory (Steely, col. 9, lines 63-65; Fig. 1, elements 108 and 116; Fig. 2A, element 221).

20. **As per claim 20**, the combination of Shen/Steely discloses the stack size decreasing (Shen, col. 5, lines 9-10) and the dirty cache line is retained in the cache memory (col. 9, lines 63-67; Fig. 1, elements 108 and 116; Fig. 2A, element 221). *It should be noted that when taking the broadest reasonable interpretation of the claim language it is clear that the limitations of the claim do not specify how much time elapses before a dirty cache line is written back to main memory (i.e. how long the dirty cache is retained in cache memory). Steely discloses that the dirty cache line will be written back into main memory at some point in time.*

21. Claims 12 and 14 are rejected under 35 U.S.C. 103(a) as being obvious over Shen et al. in view of O'Connor et al. (U.S. Patent 6,026,485) (hereinafter "O'Connor").

22. **As per claim 12**, Shen discloses all the limitations of claim 12 except an instruction decoder comprising a first portion that decodes current instructions and a second portion that decodes future instructions.

O'Connor discloses an instruction decoder comprising a first portion that decodes current instructions and a second portion that decodes future instructions (col. 3, lines

5-10, 15-18, and 42-48). *It should be noted that first instructions are current instructions while second instructions are future instructions.*

Shen and O'Connor are analogous art because they are from the same field of endeavor, that being stack-based instruction processing.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use O'Connor's instruction decoder within Shen's stack trend tracker system.

The motivation for doing so would have been to identify foldable instruction sequences and supply an execution unit with an equivalent folded operation thereby reduce processing cycles otherwise required for decoding and executing multiple operations corresponding to the multiple instructions of the folded instruction sequence (O'Connor, col. 3, lines 20-25).

Also, at the time of the invention it would have been obvious to a person of ordinary skill in the art to apply O'Connor's instruction decoder to Shen's stack trend tracker system because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded the predictable results of instruction folding for a stack based machine.

Therefore, it would have been obvious to combine O'Connor with Shen for the benefit of obtaining the invention as specified in claim 12.

23. **As per claim 14**, the combination of Shen/O'Connor discloses the second portion of the decoder is adjusted so that the number of future instructions that are

decoded equals at least two (O'Connor, col. 3, lines 59-60). *It should be noted that first instructions are current instructions while second and third instructions are both future instructions.*

Response to Arguments

24. Applicant's arguments filed December 12, 2007 with respect to **claims 1-6, 8, 11-14, and 17-20** have been fully considered but they are not persuasive.

25. With respect to Applicant's argument in the first full paragraph on page 10 of the communication filed December 12, 2007, the Examiner respectfully disagrees. Again, Applicant has failed to give an explicit definition of what "trend information" specifically entails within the specification. As commonly defined, a "trend" is "the general movement over time of a statistically detectable change." In Shen, a new stack pointer indicates the final value of the stack and therefore the new stack pointer reflects the general movement of the stack size over a period of time (the period of time being the time between the generation of the old stack pointer and the generation of the new stack pointer). Accordingly, Shen's stack pointer sufficiently discloses "determining stack trend information."

26. With respect to Applicant's argument in the first full paragraph on page 11 of the communication filed December 12, 2007, the Examiner respectfully disagrees and refers Applicant to Shen, col. 4, lines 40-43; Fig. 2, element 20, which state "increment logic 20 determines increment value 94 to add to stack pointer 12..." Paragraph 0023, lines 9-10 of Applicant's specification state "For example, trend logic 21 may receive

CURRENT 68 and FUTURE 70 to generate the trend information about the stack 32." Since a new stack pointer indicates the "trend" of the stack and the increment logic generates the new stack pointer, it follows that the increment logic generates "stack trend information." Accordingly, Shen's increment logic sufficiently discloses "trend logic."

27. With respect to Applicant's argument in the second full paragraph on page 11 of the communication filed December 12, 2007, the Examiner respectfully disagrees. As noted in the rejection above, the stack pointer, which indicates the "trend" of the stack, is utilized to prevent push/pop pairing which in turn prevents a second cache access, therefore, data traffic between various levels of the cache are reduced. Accordingly, Shen sufficiently discloses utilizing the trend information to reduce data traffic between various levels of a memory. Assuming, *in arguendo*, that Shen does not discloses this limitation, the Examiner notes that the limitation "to reduce data traffic between various levels of a memory" is merely a recitation of intended use for the "trend information." A recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim.

28. With respect to Applicant's argument in the second full paragraph on page 11 of the communication filed December 12, 2007, the Examiner respectfully disagrees. The various stages in Shen's pipelined processor contain both current and future instructions. These instructions are used to generate a new stack pointer. As detailed

above, the new stack pointer reflects the "trend" of the stack and is therefore equivalent to "trend information." Accordingly, Shen sufficiently discloses "the trend information about the stack is based on at least one future instruction."

29. With respect to Applicant's argument in the first full paragraph on page 12 of the communication filed December 12, 2007, the Examiner respectfully disagrees. The Examiner has provided "The PC Guide: The Memory Controller" (hereinafter "PC Guide") as extrinsic evidence. PC Guide clearly states that every computer has within it a hardware logic circuit called the memory controller. Also, PC Guide clearly states that the memory controller generates the necessary signals to control the reading and writing of information from and to the memory. Lastly, PC Guide clearly states that the memory controller interfaces the memory with the other major parts of the computer system. Keeping this all in mind, Shen discloses a computer in which a cache memory is read from and written to. Accordingly, Shen inherently discloses a memory controller.

30. With respect to Applicant's argument in the second full paragraph on page 12 of the communication filed December 12, 2007, the Examiner respectfully disagrees. As can be seen in Shen, col. 5, lines 10-14 and 19-22, the increment logic generates the stack pointer and the three-port adder outputs the stack pointer to the cache. As detailed in section 29 of the current Office action, Shen inherently discloses a memory controller which generates the necessary signals to control the reading and writing of information from and to the memory and also interfaces the memory with the other major parts of the computer system. Thus, any data the three-port adder outputs to the cache (i.e. the stack pointer) must also be provided to the memory controller so that it

may be properly written to the cache. Accordingly, Shen inherently discloses the trend logic provides trend information about the stack to the controller.

31. With respect to Applicant's argument on page 17 of the communication filed December 12, 2007, the Examiner respectfully disagrees. It is noted that the features upon which Applicant relies (i.e., "more than one word in the dirty cache line") are not recited in the rejected claim. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Applicant's claim simply states "which word of the dirty cache line" which can be broadly and reasonably interpreted as a dirty cache line with one word. Accordingly, the combination of Shen/Steely sufficiently discloses claim 6.

32. With respect to Applicant's argument beginning in the last full paragraph on page 18 through the first full paragraph on page 19 of the communication filed December 12, 2007, the Examiner respectfully disagrees. It is noted that the features upon which Applicant relies (i.e., "more than one word in the dirty cache line") are not recited in the rejected claim. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Applicant's claim simply states "a predetermined word within a dirty cache line" which certainly does not require a dirty cache line with more than one word. Accordingly, the combination of Shen/Steely sufficiently discloses claim 17.

33. With respect to Applicant's argument in the last full paragraph on page 19 of the communication filed December 12, 2007, the Examiner respectfully disagrees. As noted above, Shen's new stack pointer indicates the final value of the stack and therefore the new stack pointer reflects the general movement of the stack size over a period of time. In other words, the new stack pointer indicates whether the stack has incremented (i.e. increased) or decremented (i.e. decreased) since the old stack pointer was generated. Accordingly, the combination of Shen/Steely sufficiently discloses "determining whether the size of a stack is increasing or decreasing."

34. With respect to Applicant's argument in the last full paragraph on page 19 of the communication filed December 12, 2007, the Examiner respectfully disagrees and refers Applicant to the fifth paragraph of section 16 and the eighth paragraph of section 17 of the current Office action. The Examiner also notes the Supreme Court Decision in *KSR International Co. v. Teleflex Inc., 550 U.S.---, 82 USPQ2d 1385 (2007)*. According to the Supreme Court, the teaching, suggestion, motivation (TSM) test is one of a number of valid rationales that could be used to determine obviousness under 35 U.S.C. § 103. It is not the only rationale that may be relied upon to support a conclusion of obviousness. Not finding TSM does not imply non-obviousness. Assuming, *in arguendo*, that the TSM test rationale provided by the Examiner is unsatisfactory, the Examiner has provided additional rationales to support a conclusion of obviousness. Accordingly, the combination of Shen/Steely sufficiently discloses claims 19 and 20.

35. As for Applicant's arguments with respect to the dependent claims, the arguments rely on the allegation that the independent claims are allowable and

therefore for the same reasons the dependent claims are allowable. However, as addressed above, the independent claims are not allowable, thus, Applicant's arguments with respect to the dependent claims are not persuasive.

Conclusion

STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by MPEP 707.70(i):

Allowable Subject Matter

36. **Claims 7, 9, 10, 15, and 16** are allowed for the reasons set forth in the Office action dated August 22, 2006.

Claims Rejected in the Application

37. Per the instant office action, **claims 1-6, 8, 11-14, and 17-20** have received a second action on the merits and are subject of a second action final.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Arpan P. Savla whose telephone number is (571)272-1077. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on (571) 272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Arpan P. Savla/
Examiner, Art Unit 2185
March 17, 2008

/H. K./
Primary Examiner, Art Unit 2185